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UNIVERSITY of PENNSYLVANIA

PHILADELPHIA, PENNSYLVANIA 19104

Final Report

RESEARCH ON FAULT ANALYSIS OF ANALOG CIRCUITS

For Contract N00014-75-C-0768

Samuel D. Bedrosian

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

THE MAIN RESULTS OF THIS STUDY HAVE BEEN PRESENTED IN THE Ph.D. DISSERTATION OF JH LEE AUGUST 1980, WHICH INCLUDES ALGORITHMS BASED ON FUZZY DISTANCE AND ENTROPY MEASURES. THE RESULTS WITH REALISTIC CIRCUIT DIAGNOSIS HAVE BEEN QUITE PROMISING. EXTENSIONS TO EVEN MORE FLEXIBLE TECHNIQUES ARE ALSO INDICATED.

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University of Pennsylvania

The Moore School of Electrical Engineering

Systems Engineering Department

FINAL REPORT

RESEARCH ON FAULT ANALYSIS OF ANALOG CIRCUITS

Samuel D. Bedrosian

July 1982

Prepared for the
Office of Naval Research
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DISTRIBUTION STATEMENT

Final Report

Objective of This Study

The overall objective of this research project on Fault Analysis of Analog Circuits has been stated as follows:

The fact is that Naval Electronic Systems continue to become more complex. There is increasing urgency to develop equally sophisticated procedures for detection, diagnosis and prediction of system faults. There is, in fact, compelling need for excellent reliability and maintainability to make possible significant reduction in life cycly costs. Our aim is to make a viable ATE design that takes maximum advantage of inexpensive test equipment and simple computation facilities.

A simplified expression of the main thrust of the stated objective is given by the block diagram in Fig. 1 taken from one of our earlier papers [1] concerned with user's needs. See Fig. 2 for the form of learning models.

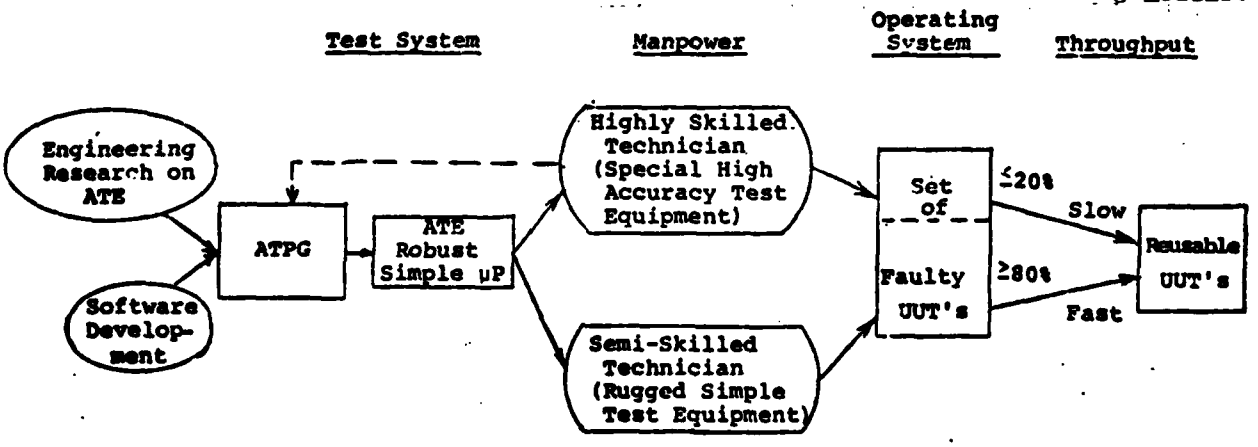


Fig. 1 Overview of System Configuration

The approach used to achieve this result involved adaptive learning models in conjunction with fuzzy set concepts. The latter helped to cut down the amount of data required to resolve ambiguities and make a decision with respect to a fault. Since statistics are often difficult if not impossible to obtain,

the fuzzy measures provide an alternative vehicle to deal with the inherent uncertainties prevalent with analog circuits and systems measurements in the presence of noise as well as component tolerances. An advantage of this technique is its versatility and potential for dealing with integrated circuit (IC) implementation.

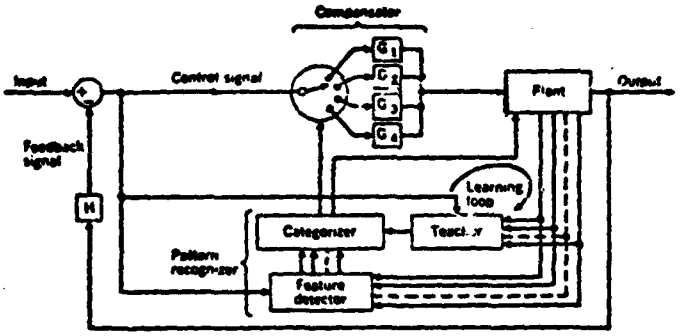
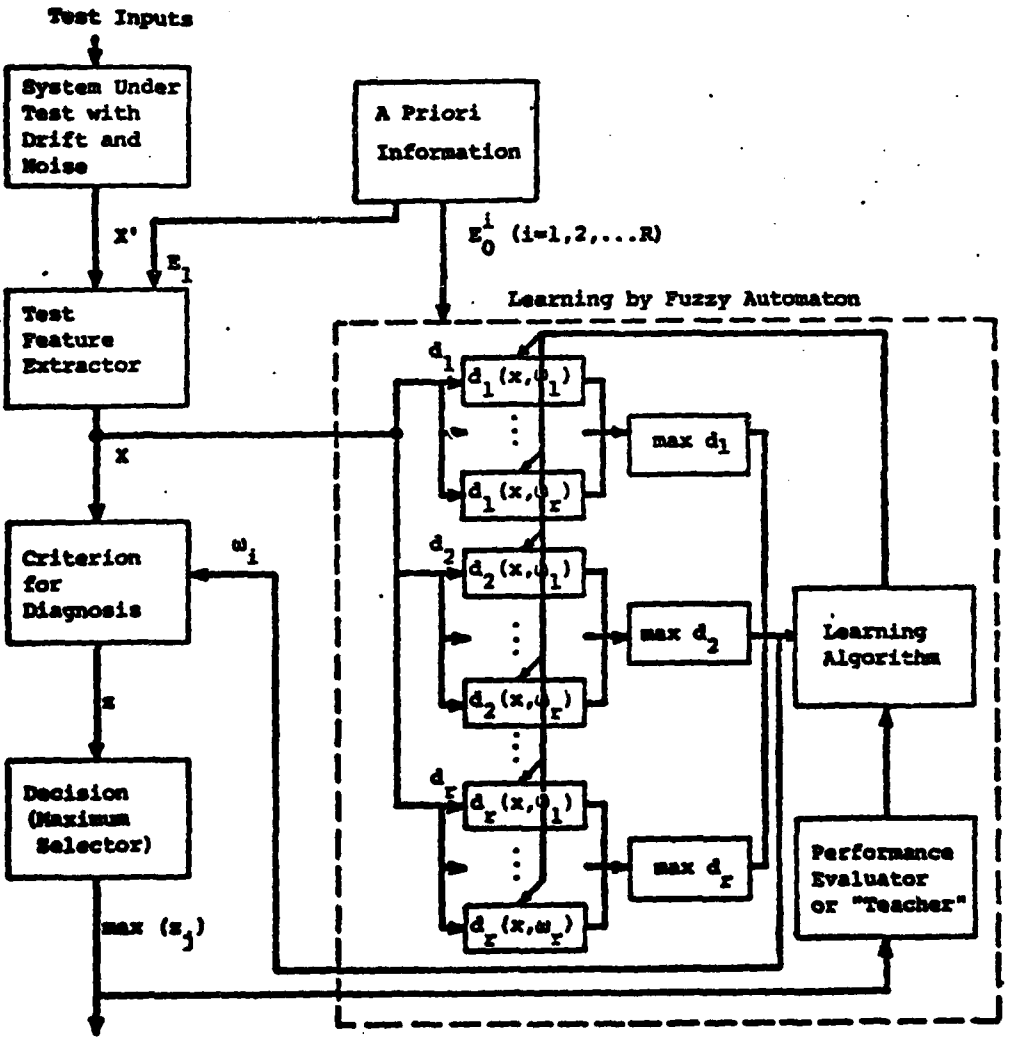


Figure 2 General form of learning control system.



ABSTRACT OF PH.D DISSERTATION

FAULT ANALYSIS OF ANALOG ELECTRONIC SYSTEMS:

Algorithms based on Fuzzy Sets

Jonghee Lee

Samuel D. Bedrosian

There are essentially three fundamental problems involved in achieving effective automatic generation of fault isolation tests for analog electronic systems: feature extraction, fault classification and diagnosis.

For practical electronic circuits having component drifts and measurement noise, how are we able to introduce fuzzy set concepts and provide methods to achieve fault classification and diagnosis?

Along with the feature extraction problem, given an electrical network of known topology, what are the conditions for testability?

To attack the long standing fault isolation problem in analog electronic circuits, we have focused on two of the major problems. One is the presence of uncertainties such as indeterminacy, vagueness, randomness, and so on that naturally arise during the solution procedure of analog fault isolation. The other is the presence of topological restrictions inherent in specific circuit configurations.

Our main attention was focused on dealing with the fault isolation problem involving various kinds of uncertainties such as indeterminacy or vagueness. We show that such problems lend themselves very well to and in fact can be solved by adopting fuzzy set concepts. In particular, this line of research has produced a modified fuzzy set technique applicable to automatic fault isolation. Topological aspects utilizing graph theory may be used effectively to assist in preanalysis of faulty analog electronic circuits. As a spin off of a consideration of these problems, we developed some new

theorems for element value solvability. It should be made clear however that effective fault isolation can be accomplished with or without this preanalysis to assist in resolving the more fundamental problem incurred by uncertainty.

As a consequence, this research yields the following specific results:

1. A base line automatic isolation system which can be used to deal with various kinds of uncertainties. A fuzzy automaton model served as a point of departure for the base line system. Various fuzzy relations are used to select and update the parameters and structures of the system.
2. Set of algorithms and new decision criteria which can be implemented easily and used for effective fault isolation. A fuzzy distance measure and a fuzzy entropy measure are used for decision making in the fault isolation algorithms. The results are shown to be generally more effective than existing techniques.
3. Ample illustrative examples and simulation studies are included to back up these new methods. Several examples such as low pass filter, band pass filter, and communication I/O circuits are used to illustrate the simulation studies. The results of simulation studies demonstrate the applicability of a fuzzy set technique.

The above outline and the discussions in several of our papers (see p.5 & 16) indicate the effort applied to this project. Copies of the dissertation were sent to those on the distribution list so our comments are kept brief
It is worth mentioning here that the efficacy of the basic approach is in the final stages of being tested by NOSC, San Diego under a separate contract.

Publications: 1978-1979

1. S. D. Bedrosian and J. H. Lee, "A Fault Isolation Method in Nonlinear Analog Networks Using Fuzzy Set Concepts," Proc. of 12th Asilomar Conference on Circuits, Systems and Computers, November 1978.

2. S. D. Bedrosian, "Analog ATPG: A Response to Users' Needs, "Proc. AUTOTESTCON '78, November 1978.

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4. S. D. Bedrosian and J. H. Lee, "Further Results on a Fuzzy Measure Function for Analog Fault Isolation," IEEE International Symposium on Circuits and Systems, Tokyo, Japan, July 1979.

5. S. D. Bedrosian and J. H. Lee, "Fault Isolation Algorithm for Analog Electronic Systems Using the Fuzzy Concept," IEEE Trans. on Circuits and Systems, Vol. CAS-26, July 1979.

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Publications: 1979-1980

1. S. D. Bedrosian and J. H. Lee, "Graph Theoretic Aspects of Analog Fault Diagnosis," Proceedings 17th Allerton Conference on Communication Control and Computing, University of Illinois, Oct. 1979.

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3. J. H. Lee, "Fault Analysis of Analog Electronic Systems: Algorithms baded on Fuzzy Sets," Ph.D. Dissertation, Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, PA, Aug. 1980.

4. S. D. Bedrosian and J. H. Lee, "Analog Fault Isolation in Non-linear Electronic Circuits with Fuzzy Learning Scheme," 1980 European Conference on Circuit Theory and Design, Warsaw, Poland, Sept. 1980.

Presentations:

5. 1979 Cherry Hill Test Conference. Panelist on Analog Fault Diagnosis, Oct. 24, 1979, Cherry Hill, New Jersey.

6. Panelist on JLC on Automatic Testing, NSIA Industry/Joint Services Automatic Testing Conference & Workshop, June 1980, San Diego, CA.

Future Directions

Looking forward to the implementation of newer electronic systems primarily with integrated circuit (IC) chips, we can also anticipate that there will be increased use of digital circuits. Two decades of effort in this direction is having a significant impact. Nevertheless, many important military electronic systems will continue to include vital analog subsystems. Therefore the very dramatic increase in density and complexity of circuitry being designed for implementation on IC chips indicates a high probability that some of them must be hybrid circuits. Another fact of life with the newer implementations is that the number of input and output pins available has not been increased commensurate with the increased component count and overall complexity of the circuits. The result of this is a crisis in the availability of test points for ATE.

This problem of test points underscores the need for serious consideration of alternatives if ATE is to remain viable and resonably effective in helping to maintain operational readiness of the sophisticated weapons systems and so forth. The perennial problem of analog fault analysis has been that the technology of circuit fabrication has been changing (and improving) faster that the ability of researchers and engineers to develop adequate ATE hardware and software along with the stubborn problem of suitable test program generation. Two important thrusts, not within the scope of this effort, are the growing appreciation for the need to plan new electronic system designs with testability in mind and the serious consideration of built-in test facilities. These need not be viewed as mutually exclusive considerations. Even those approaches will need all the help we can provide.

In the past several months we have made a start at addressing aspects of these problems. One aspect is based on the observation that the technical programs of the last few circuits and systems conferences reveal the growing significance of switched-capacitor networks (SC-networks). With the apparent pressure and rush to develop new and better SC-network designs, little if any attention has been given to the related fault analysis problem.

With the aid of a Visiting Scholar, Dr. Said I. Refai, from the Military College, Cairo, Egypt, we have developed a new flow graph technique eminently suited to the analysis of SC-networks. A general background paper has been accepted for publication in the J. Franklin Institute [5]. A second paper on the subject was written in response to an invitation to participate in the Test Techniques Session of the 1982 Large Scale Symposium October 11, 1982 [7]. That paper begins to address the diagnosis question. A third paper on SC-networks had been submitted to the 16th Asilomar Conference to be held November 1982. A copy of the Summary is included as Appendix I. Clearly much more work is needed if ATE needs are to be met.

A second aspect of the IC generated ATE problem is to recognise that use of pattern recognition techniques has not been given sufficient attention. In spite of the extremely extensive literature on pattern recognition and image processing, comparatively little has been done to enhance fault analysis for ATE. Since, in general, one has to be content with fault clusters or ambiguity groups in contrast with individual component faults for IC's innovative alternatives could very well adapt existing or new results in this area. Here again a small start has been made with images on computer terminals or in photographs in mind. Our initial effort made use of some of the back-

ground on fuzzy sets and measures developed in conjunction with Lee's 1980 Ph.D. dissertation (3). In this instance, the investigation was undertaken with a Visiting Scholar, Weixin Xie from the Northwest Telecommunication Engineering Institute in Xian, P.R.C. This has yielded a short paper in Electronics Letters [4]. Details of the development of the criterion for the number of gray levels, based on fuzzy measures, has been accepted for presentation at the First IEEE Computer Society International Symposium on Medical Imaging and Image Interpretation, to be held October 1982 in Berlin, West Germany [8].

A third approach was inspired in part by the doctoral thesis of E. Y. Chow "Failure Detection System Design Methodology" completed at MIT October, 1980. This led to a graph theoretic approach to fault detection as a term paper by Ms. Laurie Levy in the PI's graduate course on Combinatorics and Graphs. A portion of the term paper follows:

Inference systems are based in the predicate calculus and are used widely for theorem proving and deduction applications in Artificial Intelligence. A good explanation can be found in Nilsson (3).

Problem Definition

The problem, simply stated, is as follows:

Given:

1) A set of parameters, some independent (for example, physical/chemical parameters controlled in the production process of an IC chip) and some dependent (for example, electrical parameters which must meet certain test criteria).

2) Measurements of some dependent (specified) parameters, either good (pass) or bad (fail).

3) Functional relations among the parameters of the form $y = f(x_1, x_2, \ldots, x_n)$, where the x_i parameters are all causes of the parameter y (or alternately, y is the effect of $(x_1, x_2, \ldots, x_n)$).

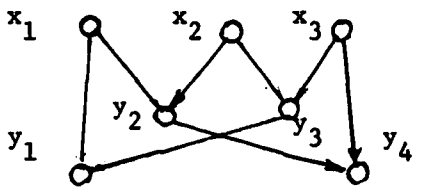
Find:

Any controlled (independent) parameters that cuases a defect (failure of a specified parameter) in the system.

The Proposed Solution

The solution approach, for the purposes of the paper, is a much more general one than most of the current research in Fault Diagnosis in Systems or Electrical Engineering. Hence of potential interest to IC implementation That we will assume is that if $y=f(x_i, \ldots, x_n)$ is bad, then some $x \in \{\ \}$

$\{x_1, \ldots, x_n\}$ causes a bad y; if $y=f(x_1, \cdots, x_n)$ is good, then all $x \in \{x_1, \ldots, x_n\}$ are good. Then the system of functional relations can be represented as a connection graph, with the nods representing the parameters and a branch for each causal relationship. Note that the graph is not necessarily 2-level, as some dependent parameters may be functions of other dependent parameters. For example, the graph shows that $\{x_1, x_2, x_3\}$



represent a set of independent parameters and $y_1 = f(x_1, y_3)$

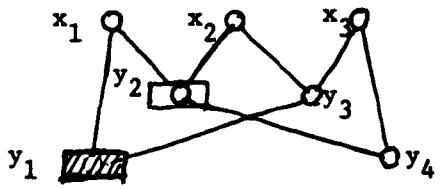
$$y_2 = f(x_1, x_2)$$

$$y_3 = f(x_2, x_3)$$

$$y_4 = f(y_2, x_3)$$

For simplicity, we will eliminate directed arrows from the graphs and assume that they are always directed downward.

Now suppose we are able to take measurements at y_1 and y_2, and the results show y_1 is bad and y_2 is good according to a predetermined criteria. We mark these results on the graph by enclosing the measured nodes in a rectangular box, and darkening in any nodes which were determined to be bad.



What now can we say about the state of the independent nodes? The diagnostic rules in the system are as follows:

Rules

1) All effects of a bad node are bad.(or equivalently, every node dependent on a bad node is bad

2) All causes of a good node must be good.

3) If a dependent node is bad, it must have at least one bad parent.

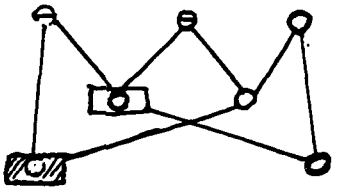
4) If all causes of a node are good, then the effect is good.

Some corollaries which follow from these rules are:

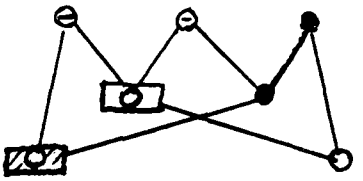
5) A node with a single cause has the same state as its cause.

6) If all causes of a bad node are good, except for one unknown cause, then the state of the unknown node is bad.

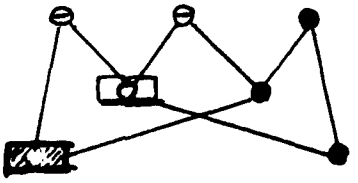
Going back to the example, we mark any node that can be derived as bad by blackening in the node, and any node that can be derived as good by putting a horizontal line through the node. The diagnosis sequence (which is not necessarily unique) and rule number of each step follows:



Rule 2.

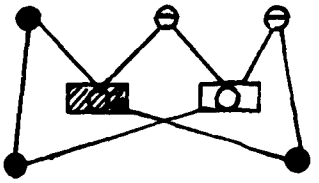


Rule 3. (applied twice)

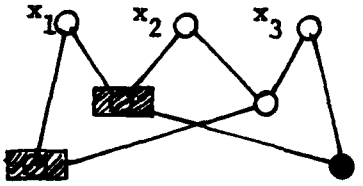


Rule 1.

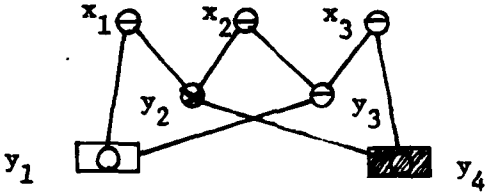
Note that this system is completely determined. That is, knowing y_1 is bad and y_2 is good, we can derive the state of each independent (top-level) node. Additional examples follow:



all nodes determined



x_1, x_2 and x_3 cannot be determined.



conflict at y_2 (see rules 3 and 4)

In the last example above, a conflict results from either the measurements at y_1 or y_2 being wrong, else there is some additional information missing from the diagram.

These examples suggest many issues in "solving" the simple networks:

Given a system in which no nodes have been tested, what is a minimal set of tests that will determine all states?

What does the structure of the network itself have to do with its determinability?

How are different structures related? Can isomorphisms be defined?

Some Preliminary Observations

Because of the logical nature of the problem, an attempt was made at devising a solution based in first order logic (i.e. using a deduction system or theorem prover to produce a solution). Many hours were spent on trying to produce a set of clauses compatable for use with a Horn Clause Theorem Prover (1) that was available for use on the Moore School Univac 1100. First, the 4 rules had to be rewritten in the predicate calculus, and then as Horn clauses.

1) $B(x) \wedge E(x,y) \rightarrow B(y)$
("if x is bad and the effect of x is y, then y is bad")

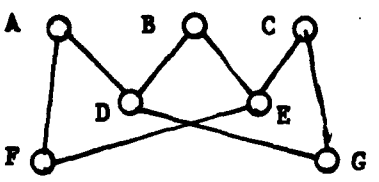
2) $G(y) \wedge E(x,y) \rightarrow g(x)$
("if y is good and the effect of x is y, then x is good")

3) $B(y) \wedge E(x,y) \wedge (E(z,y) \rightarrow G(z)) \rightarrow B(x)$
("if y is bad and the effect of x is y and all other nodes which effect y are good, then x is bad")

4) $(E(x,y) \rightarrow G(x)) \rightarrow G(y)$
("if all nodes which effect ya re good, then y is good")

The problem here is that rules 3 and 4 could not be put in Horn clause form in the time available. If an independent set of clauses can be found and written as Horn clauses, then the facts of the system would be simply which nodes are measured as good and bad and all the relations $E(x_i,x_j)$ that apply.

Another approach to solving these graphs would be to use a language such as LISP or PASCAL and write the four rules as recursive function. In LISP, the entire network could be represented as a list, and functions operating on the list could determine the causal relationships and the propagation of good and bad nodes. For example



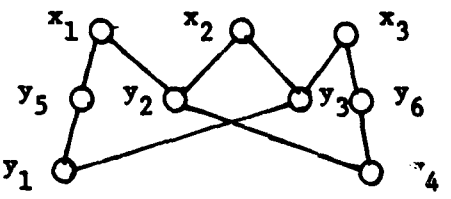
the graph could be represented as

((A F (D G))(B D (E F))(C E G))

Of course, other solution ideas are possible. Sable (5) is developing a PASCAL program which enables the user to interactively enter the network, test and make changes to system. His main area of research is incorporating Friedman's work in plausible inference (2) This allows measures of belief such as credibility, doubt and plausibility to be applied so that one is not confined only to measures or true or falso (i.e. good and bad) in the system. Mathematicians who have studied reasoning under uncertainty include Shafer (6) and Polya (4). Future research in applying their theories to our simple fault diagnosis problem would prove interesting.

Structure

First, let us examine these networks in terms of their physical structure. Note that there can be no horozontal edges in the graph (else there is no cause/effect relation) and each node of the graph belongs to a certain generation of descendants of the independent (top-level) nodes. For clarity, from now on all nodes of the same generation will be drawn at the same level. Given corollary 5, our original example can be redrawn as



without changing the logic of the system.

We can now define an isomorphism on these graphs:

> Two graphs, $\mathcal{A}$ and $\mathcal{B}$, are isomorphic if and only if there is a one-to-one and onto mapping $h: \mathcal{A} \rightarrow \mathcal{B}$ between the independent nodes of $\mathcal{A}$ and $\mathcal{B}$ and there is a mapping between the bottom-level nodes of $\mathcal{A}$ and $\mathcal{B}$ (not necessarily one-to one) which preserves the truth values of the system.

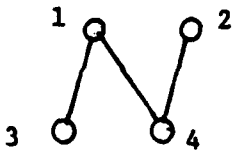


Fig. 2a

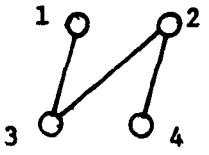


Fig. 2b

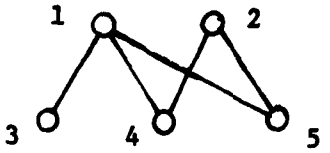


Fig. 2c

For example, figures 2a and 2b are obviously isomorphic, but so are 2a and 2c.

An algorithm developed for solving a network is easily programmed in LISP, which handles recursive tree searches easily. Other algorithms using boolean logic or spanning trees may be possible but have not been fully explored at this point. This preliminary work has shown that these simple diagnosis graphs have some interesting properties and applications where further research may prove enlightening.

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Presentations

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[10] S. D. Bedrosian, Panalist on "Future Directions in Analog Fault Diagnosis" Workshop Univ. of Notre Dame, May 1981.

Appendix I
(Submitted for 16th Asilomar Conf. Nov. 1982)

Flow Graph Technique for Analysis & Synthesis of Switched-Capacitor Networks

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Summary

The analysis of the SC-networks had been established by many methods [1,2,3,4]. In this paper we introduce the recently developed RMC-graph [5] application to the n-phase clock SC-networks that may include independent and dependent voltage (current) sources. The graph represents the Z-transform system of nodal charge equations characterising the SC-network. There are many advantages gained by application of the RMC graph to SC-networks: (1) The graph theoretic transformation within RMC-graph technique facilitates dealing with the switching function as well as dependent sources included in the SC-network (2) Also the RMC-graph can be obtained directly from the given SC-network. In particular this new flow graph technique permits analysis without the need either for a preliminary equivalent circuit [4] or SC-building blocks [2,3]. (3) This RMC-graph technique is applicable to general n-phase clock SC-network. From the "resultant" graph it is simple to obtain any network function by using the graph gain formulas. Furthermore, the great similarity between the graph and network structure enables us to derive an equivalent circuit, of the given SC-network, from the "resultant" RMC-graph obtained as indicated in Fig. 1.

The given SC-network can be treated as a superposition of three components. One component is the all capacitor network (c-network), the second consists

of an array of switches (S-network) and the third component is the ideal active transformation network (AT-network) such as the OA's, VCVS's or impedance converters.

The RMC-graph construction procedure can be schematically represented as shown in Fig. 1, and can be summarized as follows:

1 - To consider at first the original c-network. Then, in the graph we assign a node corresponding to each phase of the independent nodal voltages of the C-network. The original subgraph, which represents the nodal charge equations of the c-network is then constructed. Here it is important to mention that we avoid the delay property (i.e. all capacitors, in this step, are considered with erased memory). Thus, the original subgraph is simply and directly derived.

2 - The S-network action is considered in this step. The switching operations are graphically interpreted by a switching transformation subgraph (shown by dashed lines) that represents the transofmration equations due to switching action. The delay property which is dependant on the switching operation is now defined. The delay transformation branches (shown by dash-dot lines) is superimposed graphically. Together these comprise the transformation subgraph. Note that both are derived by inspection.

3 - A standard AT-network transformation subgraph is constructed by joining the related corresponding nodes.

4 - From original and transformation subgraphs, it is easy to determine the resultant subgraph representing the given SC-network. The applied transformation graph rules are direct [5]

In the work, several examples of SC-network blocks and their corresponding RMC-graph in Z-domain are included. Fig. 2.a shows an illustrative example of a two-phase clock SC-network (bilinear floating resister). The RMC-graph

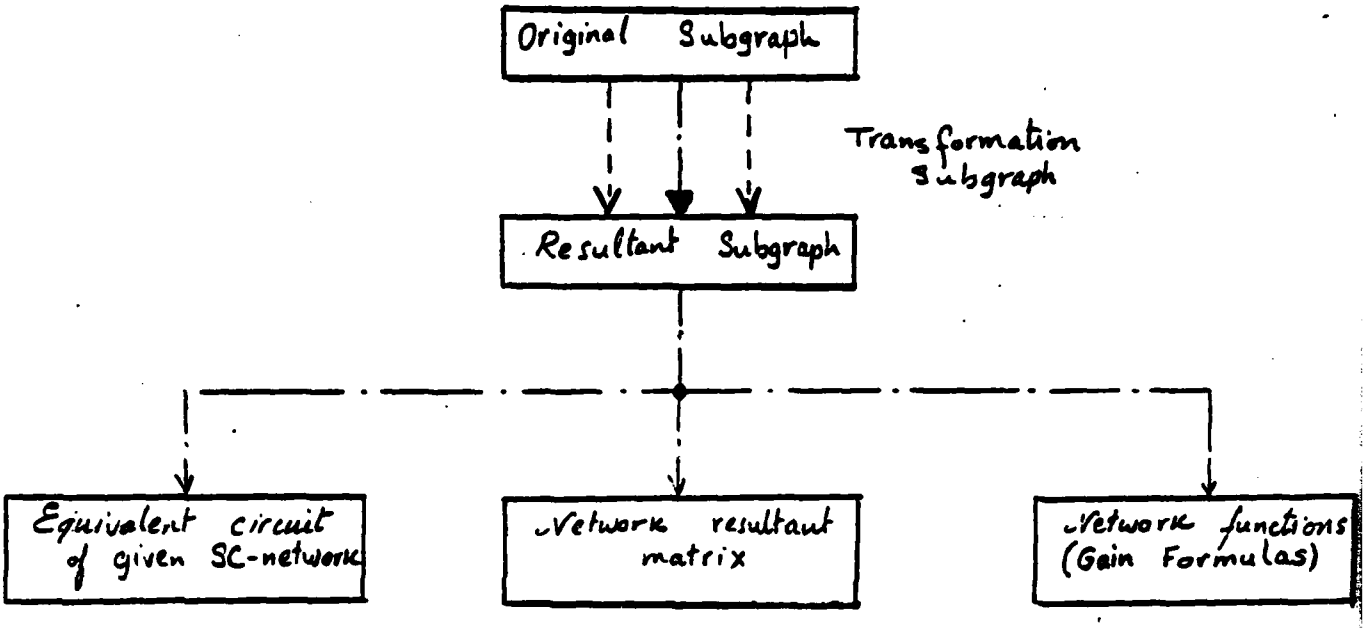

Original Subgraph
Transformation Subgraph
Resultant Subgraph
Equivalent circuit of given SC-network
Network resultant matrix
Network functions (Gain Formulas)

Fig. 1.

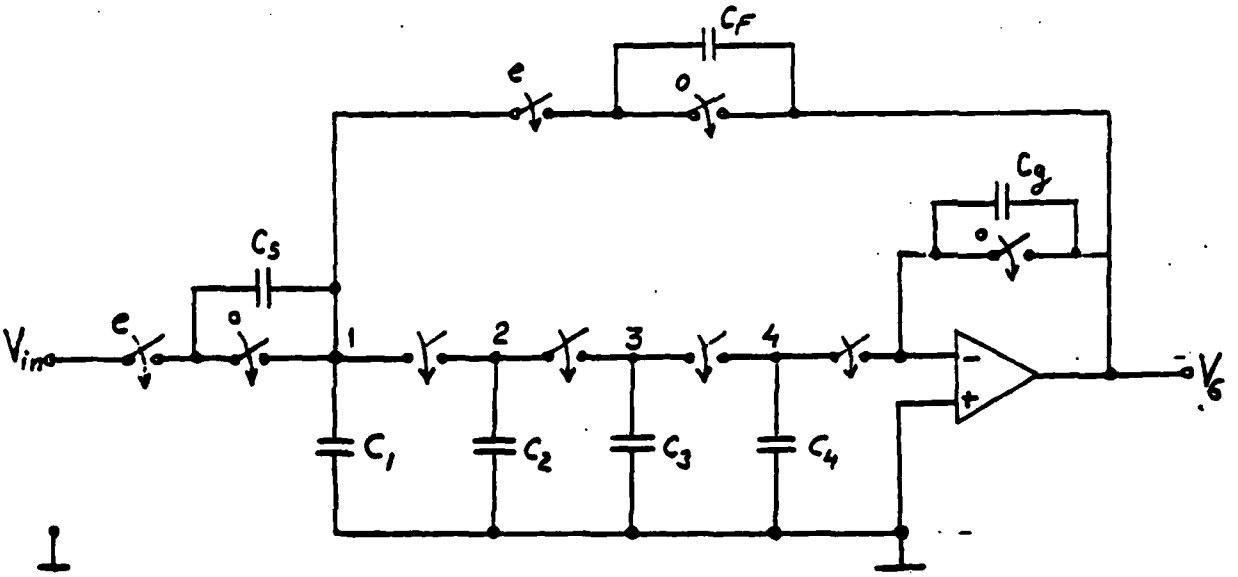
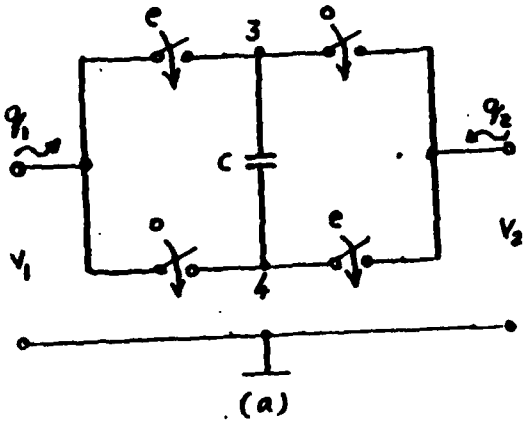
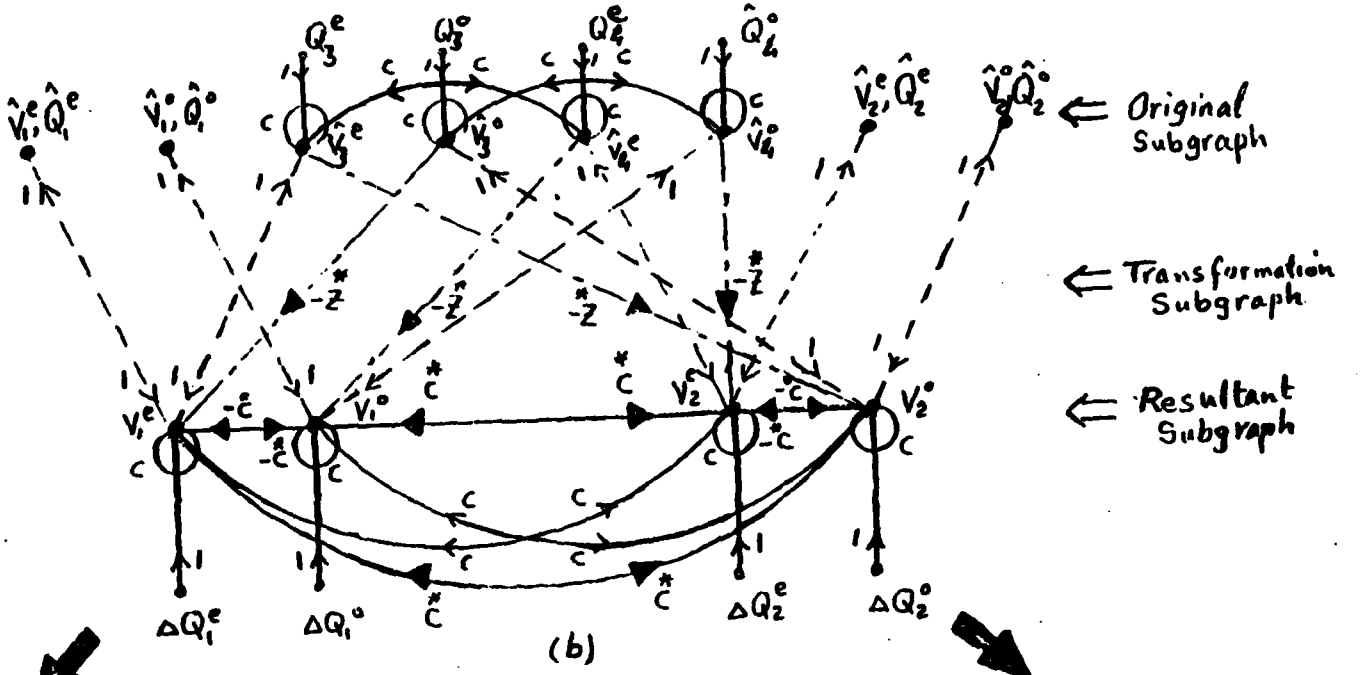

C_F
e
o
C_g
C_s
V_{in}
e
o
1
2
3
4
C_1
C_2
C_3
C_4
V_6

Fig. 3.

BILINEAR FLOATING RESISTOR



(a)

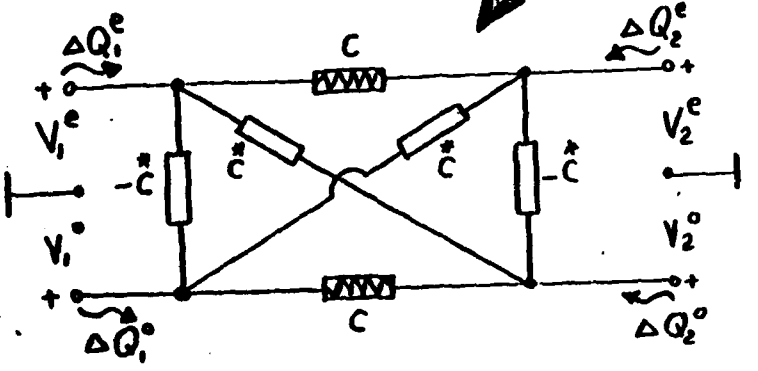


⇐ Original Subgraph

⇐ Transformation Subgraph

⇐ Resultant Subgraph

(b)



(c) EQUIVALENT CIRCUIT

$$\begin{bmatrix} \Delta Q_1^e \\ \Delta Q_1^o \\ \Delta Q_2^e \\ \Delta Q_2^o \end{bmatrix} = \begin{bmatrix} C & \overset{*}{C} & -C & -\overset{*}{C} \\ \overset{*}{C} & C & -\overset{*}{C} & -C \\ -C & -\overset{*}{C} & C & \overset{*}{C} \\ -\overset{*}{C} & -C & \overset{*}{C} & C \end{bmatrix} \cdot \begin{bmatrix} V_1^e \\ V_1^o \\ V_2^e \\ V_2^o \end{bmatrix}$$

(d) RESULTANT MATRIX

Fig. 2. $\left(\overset{*}{z} = \overset{-1/2}{z} \;,\; \overset{*}{C} = C\overset{*}{z}\right)$

of the network shown in Fig. 2.a is presented in Fig. 2.b. We can easily distinguish how much of a short-cut this direct RMC-graph technique really is. In Fig. 2c and d are introduced the equivalent circuit and the corresponding matrix which are easily derived from the "resultant" RMC-subgraph.

The RMC-graph method is further illustrated by application to the SC-network shown in Fig. 3. The simple direct graph method should be compared with the equivalent four-part network method used by Kurth [2] for the same network.

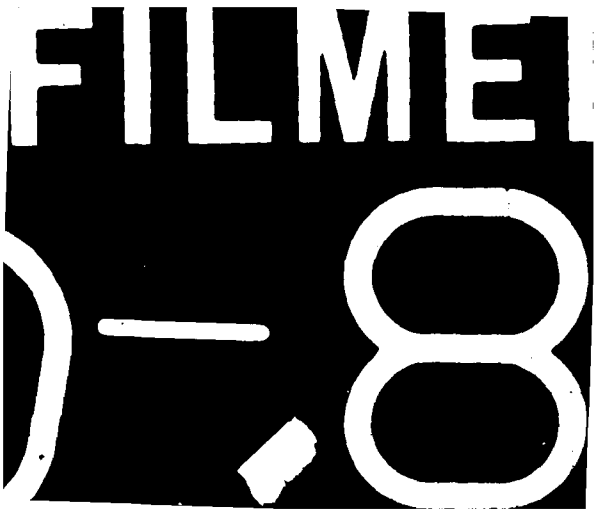
[1] M. S. Ghausi and K. R. Laker, Modern Filter Design; Active RC and Switched-Capacitor; Prentice-Hall, Inc. 1981

[2] C. F. Kurth, and G. S. Moschytz "Nodal Analysis of Switched-Capacitor Networks", IEEE Trans., 1979, CAS-26, pp. 93-105.

[3] C. F. Kurth, and G. S. Moschytz "Two-Part Analysis of Switched-Capacitor Networks Using Four-Part Equivalent Circuits in the Z-Domain", IEEE Trans., 1979, CAS-26, pp. 166-180.

[4] Jan J. Mulawka "By-Inspection Analysis of Swiched-Capacitor Networks", Int. J. Electron, 1980, 49, pp. 359-373.

[5] S. D. Bedrosian, and Said Refai "A Flow Graph Transformation Technique Specifically for Discrete Time Networks" to be published J. Franklin Inst., 1982.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